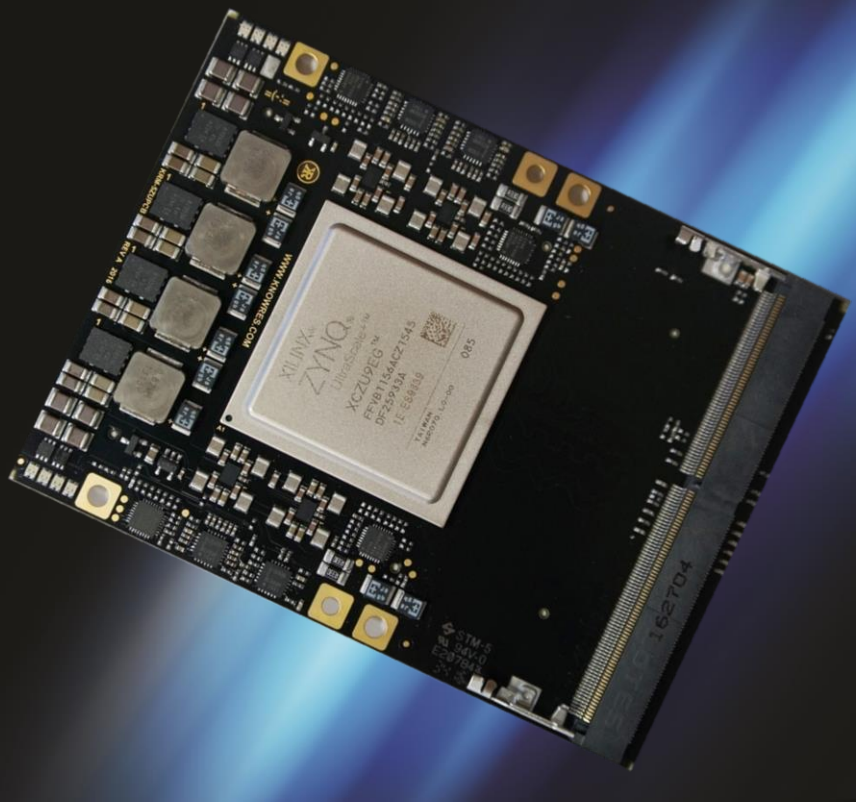
KNOWLEDGE RESOURCES
Switzerland GmbH

# KRM-5ZU9EG

- Xilinx MPSoC ZU9EG
- Ultrascale+ Fabric
- 208 HP I/O
- 72 HD I/O
- 52 PS MIO
- 24+4 GTX/GTR transceivers
- up to 16GB ECC DDR4 RAM
- eMMC & QSPI
- 12V supply



## Core component:

- Xilinx XCZU9EG-xxFFVB1156x

## Processing system:

- Quad Core ARM Cortex™- A53
- Dual Core ARM Cortex™-R5
- Mali 400 GPU

## FPGA fabric:

- Xilinx Ultrascale+™ fabric
- 274k 6-input LUT
- 548k flip flops
- 32.1MB BRAM
- 2520 DSP slices

## Memory options:

- 72 bit DDR4 SODIMM to 16GB
- eMMC to 64GB
- QSPI to 256MB

## Module I/O:

- 208 HP I/O (4 banks to 1V8)
- 72 HD I/O (3 banks to 3V3)
- 52 PS MIO (2 banks to 3V3)
- 24 GTX transceivers to 16Gb/s
  - 2 external reference inputs
  - 6 Internally generated ref clocks
- 4 PS GTP transceivers to 6.6 Gb/s
  - 1 external reference input
  - 4 internally generated ref clocks
- Master clock IN/OUT 33.333 MHz
- BMC UART
- BMC I/O
  - Module ready
  - Boot mode select
  - User function with custom FW
- JTAG
- RESET in

## Power:

- 2 separate 12V inputs
  - Split load (balanced)
  - Redundant supply (A or B)
- 3V3 Aux output
  - 1A supply max
- 1V8 Aux output
  - 1A supply max

## Clocking:

- 1: 14 clock tree
  - All module elements can be derived from one master clock
  - External clock or on-board master oscillator
- Separate clock generator per GTX column
  - Reference from master clock
  - Reference from external input
  - Up to 4 different clocks per 12 GTX
- Separate clock generator for PS GTR
  - Reference from master clock
  - Reference from external input
  - 4 clocks, one per GTR

## BMC :

- Board Management Controller for
  - Clock configuration
  - Power sequencing
  - Boot mode selection
  - Status signalling

## Dimensions:

- 100x75 mm
- 15mm max. height with heat-spreader

## Environmental:

- Extended temperature or Industrial temperature range

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